

MSM511000C/CL**1,048,576-Word × 1-Bit DYNAMIC RAM : FAST PAGE MODE TYPE****DESCRIPTION**

The MSM511000C/CL is a 1,048,576-word × 1-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM511000C/CL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM511000C/CL is available in a 26/20-pin plastic SOJ or 20-pin plastic ZIP. The MSM511000CL (the low-power version) is specially designed for lower-power applications.

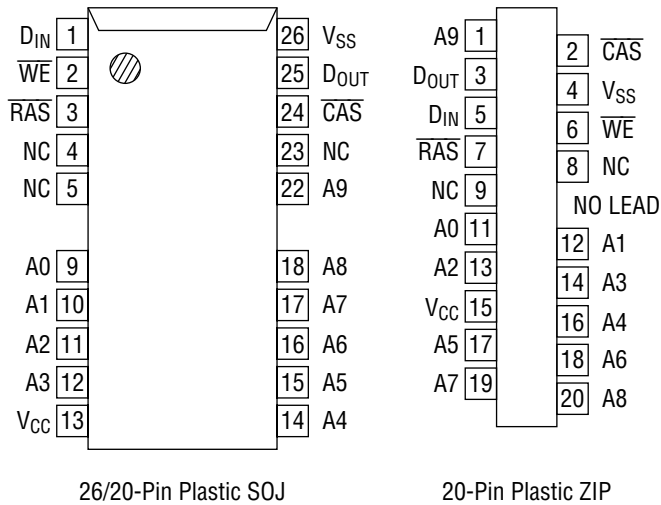
FEATURES

- 1,048,576-word × 1-bit configuration
 - Single 5 V power supply, ±10% tolerance
 - Input : TTL compatible, low input capacitance
 - Output : TTL compatible, 3-state
 - Refresh : 512 cycles/8 ms, 512 cycles/64 ms (L-version)
 - Fast page mode, read modify write capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
 - Package options:
 - 26/20-pin 300 mil plastic SOJ (SOJ26/20-P-300-1.27) (Product : MSM511000C/CL-xxJS)
 - 20-pin 400 mil plastic ZIP (ZIP20-P-400-1.27) (Product : MSM511000C/CL-xxZS)
- xx indicates speed rank.

PRODUCT FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation | |
|------------------|--------------------|-----------------|------------------|-------------------|-------------------|-------------------------------|
| | t _{RAC} | t _{AA} | t _{CAC} | | Operating (Max.) | Standby (Max.) |
| MSM511000C/CL-45 | 45 ns | 24 ns | 14 ns | 90 ns | 468 mW | 5.5 mW/ 1.1 mW (L-version) |
| MSM511000C/CL-50 | 50 ns | 26 ns | 14 ns | 100 ns | 440 mW | |
| MSM511000C/CL-60 | 60 ns | 30 ns | 15 ns | 120 ns | 385 mW | |
| MSM511000C/CL-70 | 70 ns | 35 ns | 20 ns | 130 ns | 330 mW | |

PIN CONFIGURATION (TOP VIEW)

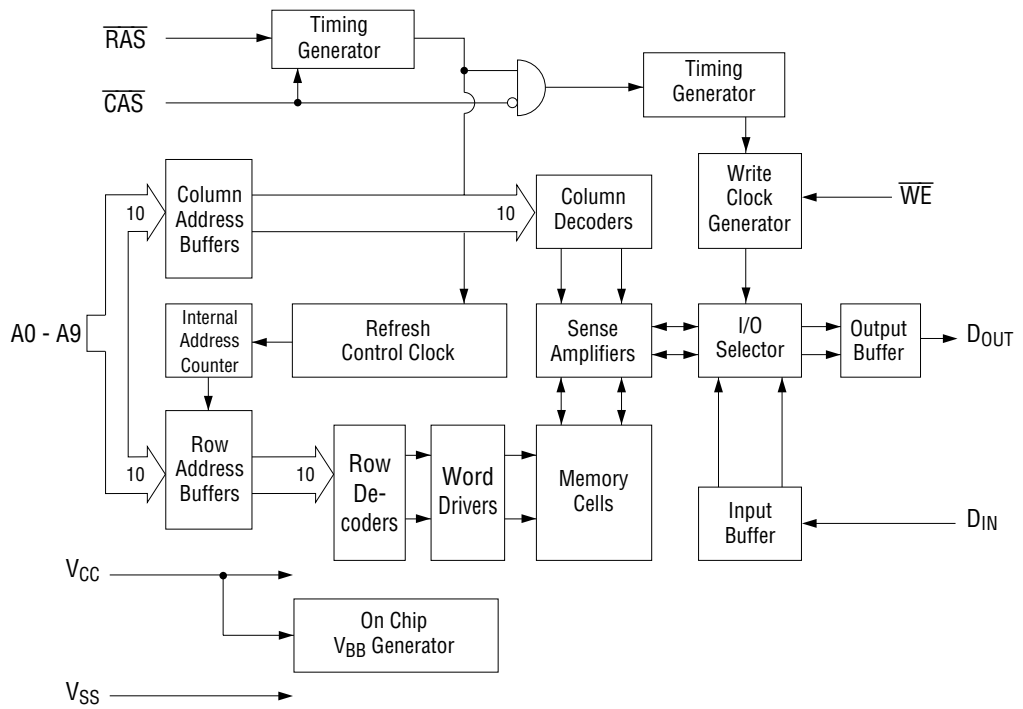


26/20-Pin Plastic SOJ

20-Pin Plastic ZIP

| Pin Name | Function |
|------------------|-----------------------|
| A0 - A9 | Address Input |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| D _{IN} | Data Input |
| D _{OUT} | Data Output |
| WE | Write Enable |
| V _{CC} | Power Supply (5 V) |
| V _{SS} | Ground (0 V) |
| NC | No Connection |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|-----------|-------------|------|
| Voltage on Any Pin Relative to V_{SS} | V_T | -1.0 to 7.0 | V |
| Short Circuit Output Current | I_{OS} | 50 | mA |
| Power Dissipation | P_D^* | 1 | W |
| Operating Temperature | T_{opr} | 0 to 70 | °C |
| Storage Temperature | T_{stg} | -55 to 150 | °C |

*: $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

($T_a = 0^\circ\text{C}$ to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|----------|------|------|------|------|
| Power Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V_{IH} | 2.4 | — | 6.5 | V |
| Input Low Voltage | V_{IL} | -1.0 | — | 0.8 | V |

Capacitance

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|-----------|------|------|------|
| Input Capacitance ($A_0 - A_9, D_{IN}$) | C_{IN1} | — | 5 | pF |
| Input Capacitance ($\overline{RAS}, \overline{CAS}, \overline{WE}$) | C_{IN2} | — | 5 | pF |
| Output Capacitance (D_{OUT}) | C_{OUT} | — | 6 | pF |

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C to } 70^\circ\text{C}$)

| Parameter | Symbol | Condition | MSM511000 C/CL-45 | | MSM511000 C/CL-50 | | MSM511000 C/CL-60 | | MSM511000 C/CL-70 | | Unit | Note |
|--|------------|--|---------------------|----------|---------------------------|------|-------------------|------|-------------------|------|---------------|---------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| | | | Output High Voltage | V_{OH} | $I_{OH} = -5.0\text{ mA}$ | 2.4 | V_{CC} | 2.4 | V_{CC} | 2.4 | | |
| Output Low Voltage | V_{OL} | $I_{OL} = 4.2\text{ mA}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | I_{LI} | $0\text{ V} \leq V_i \leq 6.5\text{ V}$; All other pins not under test = 0 V | -10 | 10 | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Output Leakage Current | I_{LO} | D_{OUT} disable $0\text{ V} \leq V_o \leq 5.5\text{ V}$ | -10 | 10 | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Average Power Supply Current (Operating) | I_{CC1} | $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$ | — | 85 | — | 80 | — | 70 | — | 60 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC2} | $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ | — | 2 | — | 2 | — | 2 | — | 2 | mA | 1 |
| | | $\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$ | — | 1 | — | 1 | — | 1 | — | 1 | μA | 1, 5 |
| | | | — | 200 | — | 200 | — | 200 | — | 200 | μA | |
| Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh) | I_{CC3} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$ | — | 85 | — | 80 | — | 70 | — | 60 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC5} | $\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, $D_{OUT} = \text{enable}$ | — | 5 | — | 5 | — | 5 | — | 5 | mA | 1 |
| Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh) | I_{CC6} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ | — | 85 | — | 80 | — | 70 | — | 60 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | I_{CC7} | $\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$ | — | 80 | — | 75 | — | 65 | — | 55 | mA | 1, 3 |
| Average Power Supply Current (Battery Backup) | I_{CC10} | $t_{RC} = 125\ \mu\text{s}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, $t_{RAS} \leq 1\ \mu\text{s}$ | — | 300 | — | 300 | — | 300 | — | 300 | μA | 1, 4, 5 |

- Notes :
- I_{CC} Max. is specified as I_{CC} for output open condition.
 - The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 - The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 - $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $-1.0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.
 - L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

| Parameter | Symbol | MSM511000 C/CL-45 | | MSM511000 C/CL-50 | | MSM511000 C/CL-60 | | MSM511000 C/CL-70 | | Unit | Note |
|--|-------------------|----------------------|---------|----------------------|---------|----------------------|---------|----------------------|---------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | t _{RC} | 90 | — | 100 | — | 120 | — | 130 | — | ns | |
| Read Modify Write Cycle Time | t _{RWC} | 110 | — | 120 | — | 140 | — | 155 | — | ns | |
| Fast Page Mode Cycle Time | t _{PC} | 34 | — | 36 | — | 40 | — | 45 | — | ns | |
| Fast Page Mode Read Modify Write Cycle Time | t _{PRWC} | 54 | — | 56 | — | 60 | — | 70 | — | ns | |
| Access Time from $\overline{\text{RAS}}$ | t _{RAC} | — | 45 | — | 50 | — | 60 | — | 70 | ns | 4, 5, 6 |
| Access Time from $\overline{\text{CAS}}$ | t _{CAC} | — | 14 | — | 14 | — | 15 | — | 20 | ns | 4, 5 |
| Access Time from Column Address | t _{AA} | — | 24 | — | 26 | — | 30 | — | 35 | ns | 4, 6 |
| Access Time from $\overline{\text{CAS}}$ Precharge | t _{CPA} | — | 28 | — | 30 | — | 35 | — | 40 | ns | 4 |
| Output Low Impedance Time from $\overline{\text{CAS}}$ | t _{CLZ} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 4 |
| $\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time | t _{OFF} | 0 | 14 | 0 | 14 | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | t _T | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | t _{REF} | — | 8 | — | 8 | — | 8 | — | 8 | ms | |
| Refresh Period (L-version) | t _{REF} | — | 64 | — | 64 | — | 64 | — | 64 | ms | |
| $\overline{\text{RAS}}$ Precharge Time | t _{RP} | 35 | — | 40 | — | 50 | — | 50 | — | ns | |
| $\overline{\text{RAS}}$ Pulse Width | t _{RAS} | 45 | 10,000 | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode) | t _{RASP} | 45 | 100,000 | 50 | 100,000 | 60 | 100,000 | 70 | 100,000 | ns | |
| $\overline{\text{RAS}}$ Hold Time | t _{RSH} | 14 | — | 14 | — | 15 | — | 20 | — | ns | |
| $\overline{\text{CAS}}$ Precharge Time (Fast Page Mode) | t _{CP} | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{CAS}}$ Pulse Width | t _{CAS} | 14 | 10,000 | 14 | 10,000 | 15 | 10,000 | 20 | 10,000 | ns | |
| $\overline{\text{CAS}}$ Hold Time | t _{CSH} | 45 | — | 50 | — | 60 | — | 70 | — | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | t _{CRP} | 5 | — | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | t _{RHCP} | 28 | — | 30 | — | 35 | — | 40 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | t _{RCD} | 17 | 31 | 18 | 36 | 20 | 45 | 20 | 50 | ns | 5 |
| $\overline{\text{RAS}}$ to Column Address Delay Time | t _{RAD} | 12 | 21 | 13 | 24 | 15 | 30 | 15 | 35 | ns | 6 |
| Row Address Set-up Time | t _{ASR} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | t _{RAH} | 7 | — | 8 | — | 10 | — | 10 | — | ns | |
| Column Address Set-up Time | t _{ASC} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | t _{CAH} | 12 | — | 13 | — | 15 | — | 15 | — | ns | |
| Column Address Hold Time from $\overline{\text{RAS}}$ | t _{AR} | 35 | — | 40 | — | 50 | — | 55 | — | ns | |
| Column Address to $\overline{\text{RAS}}$ Lead Time | t _{RAL} | 24 | — | 26 | — | 30 | — | 35 | — | ns | |

AC Characteristics (2/2)

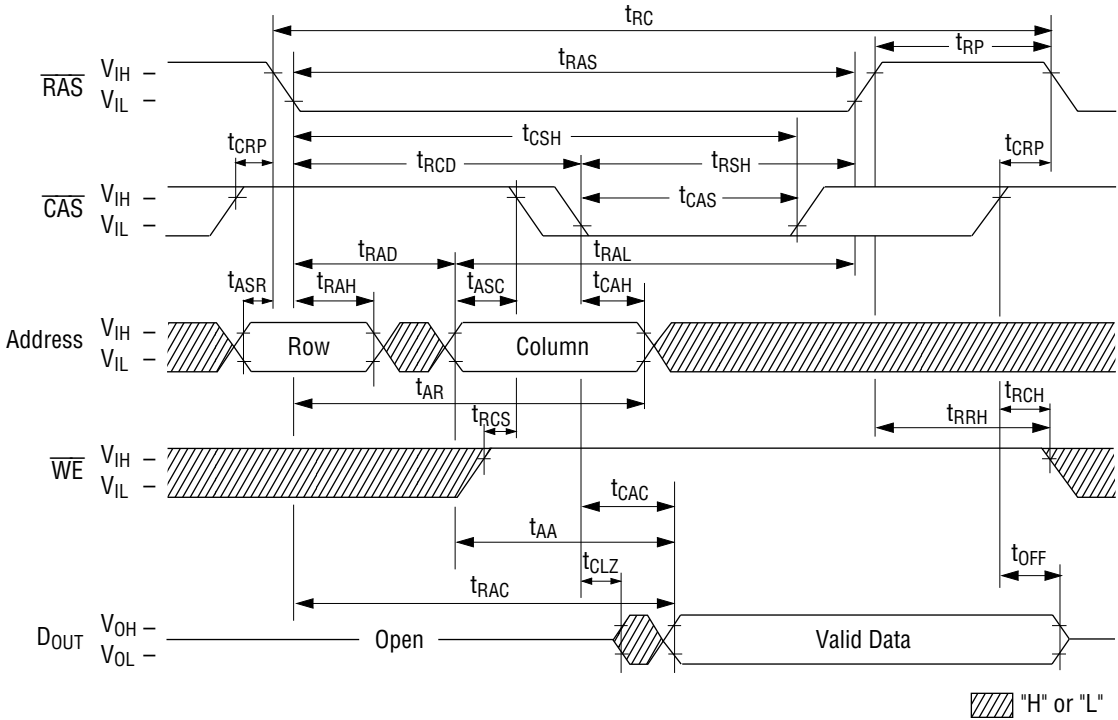
(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

| Parameter | Symbol | MSM511000 C/CL-45 | | MSM511000 C/CL-50 | | MSM511000 C/CL-60 | | MSM511000 C/CL-70 | | Unit | Note |
|---|-------------------|----------------------|------|----------------------|------|----------------------|------|----------------------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read Command Set-up Time | t _{RCS} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time | t _{RCH} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{\text{RAS}}$ | t _{RRH} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 8 |
| Write Command Set-up Time | t _{WCS} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | t _{WCH} | 10 | — | 10 | — | 10 | — | 15 | — | ns | |
| Write Command Hold Time from $\overline{\text{RAS}}$ | t _{WCR} | 35 | — | 40 | — | 50 | — | 55 | — | ns | |
| Write Command Pulse Width | t _{WP} | 10 | — | 10 | — | 10 | — | 15 | — | ns | |
| Write Command to $\overline{\text{RAS}}$ Lead Time | t _{RWL} | 14 | — | 14 | — | 15 | — | 20 | — | ns | |
| Write Command to $\overline{\text{CAS}}$ Lead Time | t _{CWL} | 14 | — | 14 | — | 15 | — | 20 | — | ns | |
| Data-in Set-up Time | t _{DS} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 10 |
| Data-in Hold Time | t _{DH} | 12 | — | 13 | — | 15 | — | 15 | — | ns | 10 |
| Data-in Hold Time from $\overline{\text{RAS}}$ | t _{DHR} | 35 | — | 40 | — | 50 | — | 55 | — | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | t _{CWD} | 14 | — | 14 | — | 15 | — | 20 | — | ns | 9 |
| Column Address to $\overline{\text{WE}}$ Delay Time | t _{AWD} | 24 | — | 26 | — | 30 | — | 35 | — | ns | 9 |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | t _{RWD} | 45 | — | 50 | — | 60 | — | 70 | — | ns | 9 |
| $\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time | t _{CPWD} | 33 | — | 35 | — | 40 | — | 45 | — | ns | 9 |
| $\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge | t _{RPC} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{CSR} | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{CHR} | 25 | — | 25 | — | 30 | — | 30 | — | ns | |

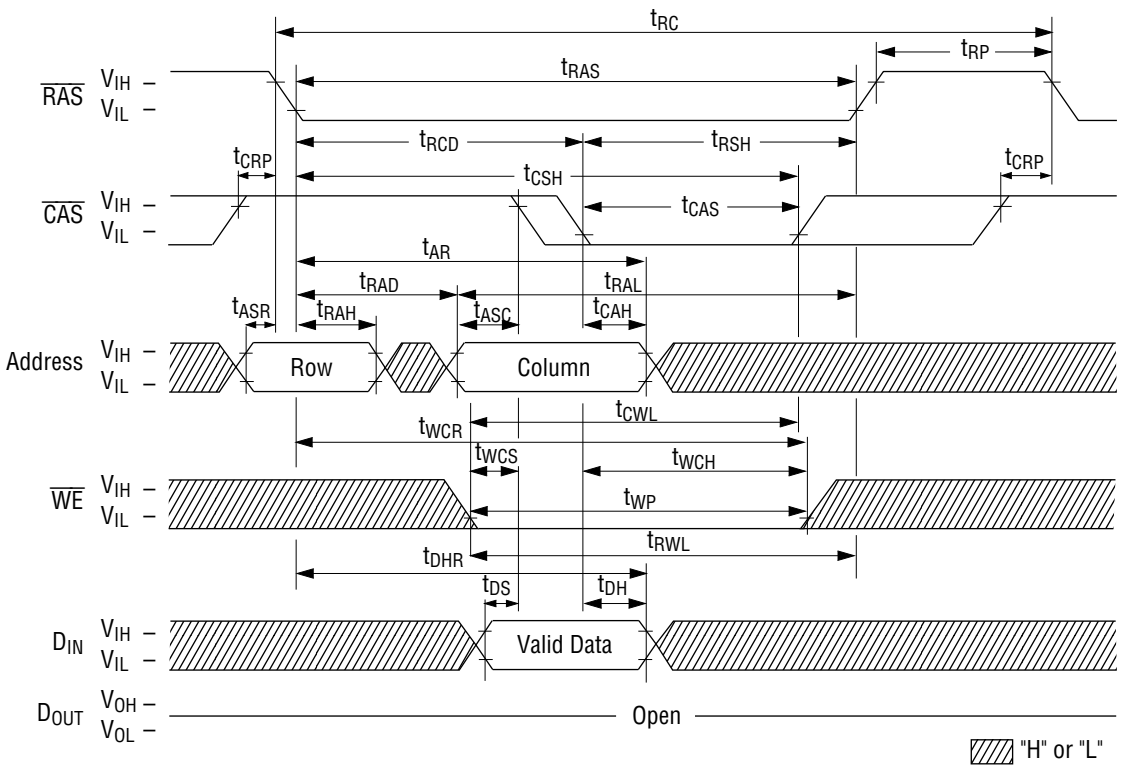
- Notes:
1. A start-up delay of 100 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in a read modify write cycle.

TIMING WAVEFORM

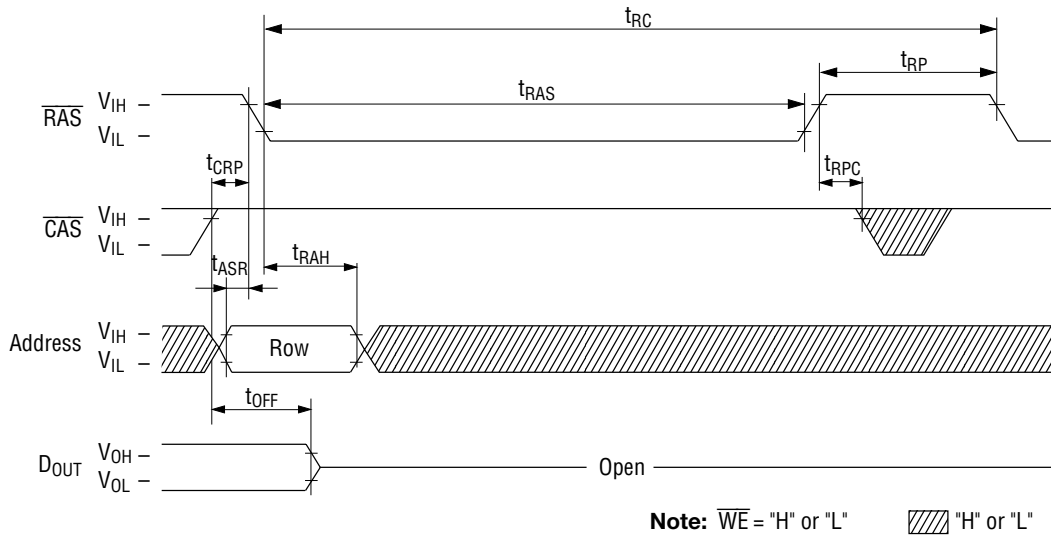
Read Cycle



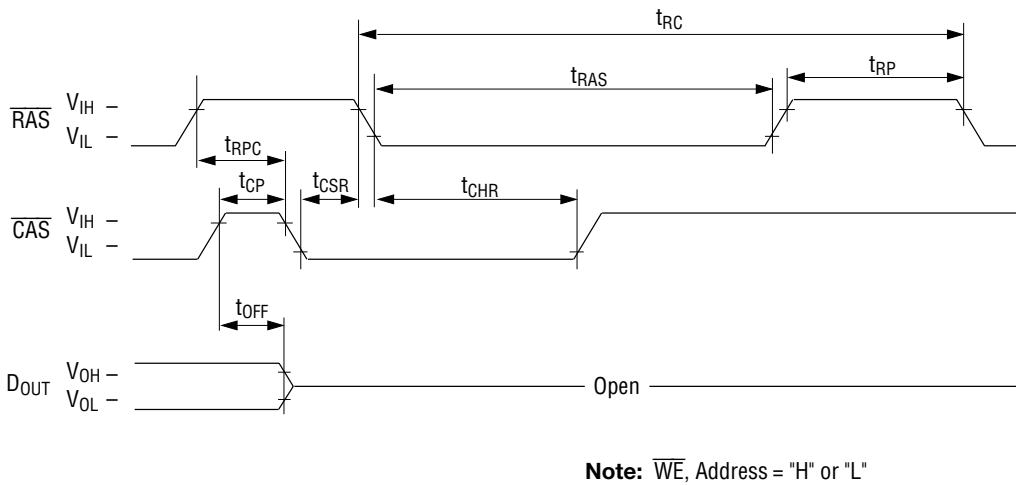
Write Cycle (Early Write)



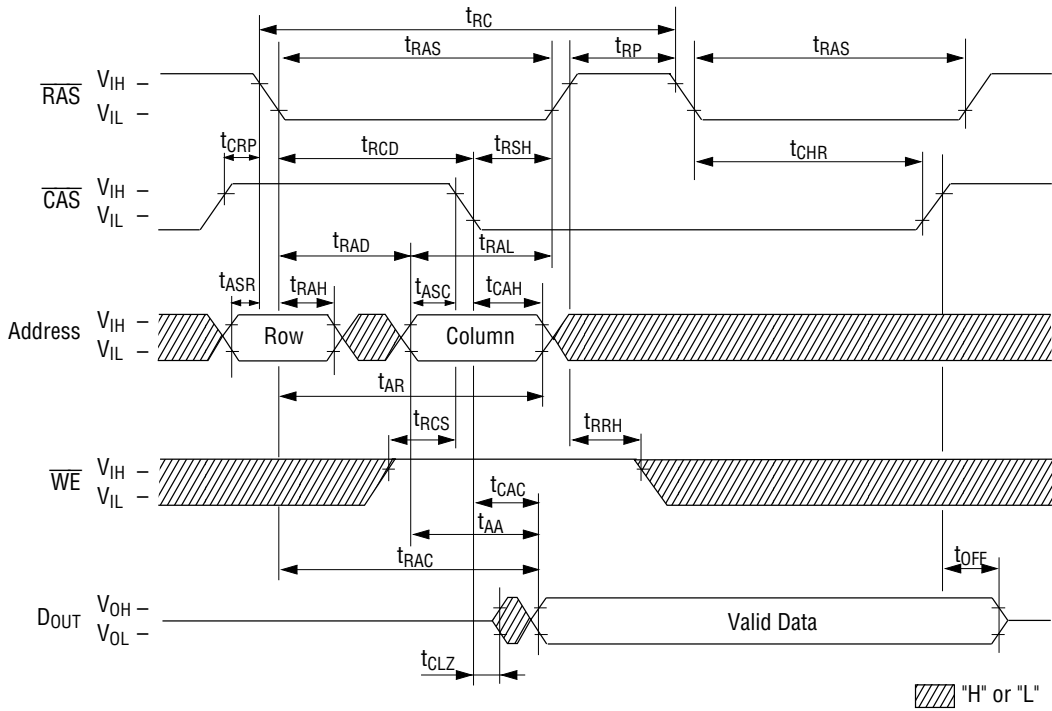
RAS-Only Refresh Cycle



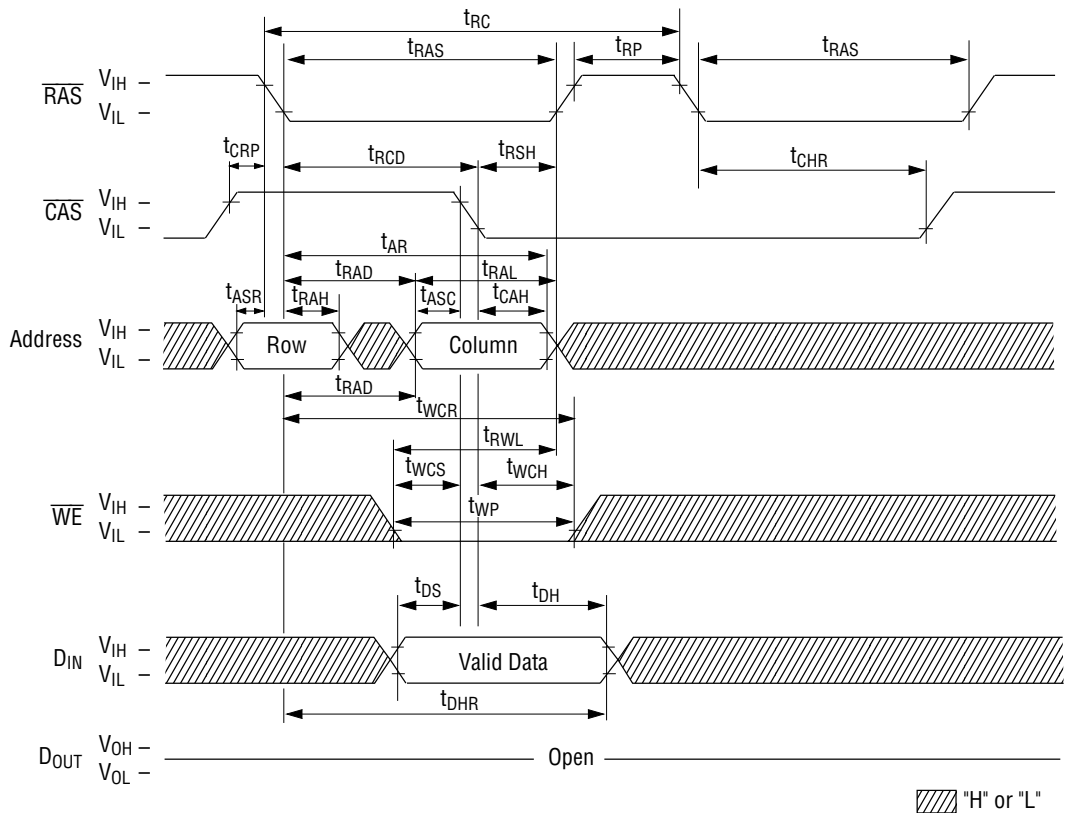
CAS before RAS Refresh Cycle



Hidden Refresh Read Cycle

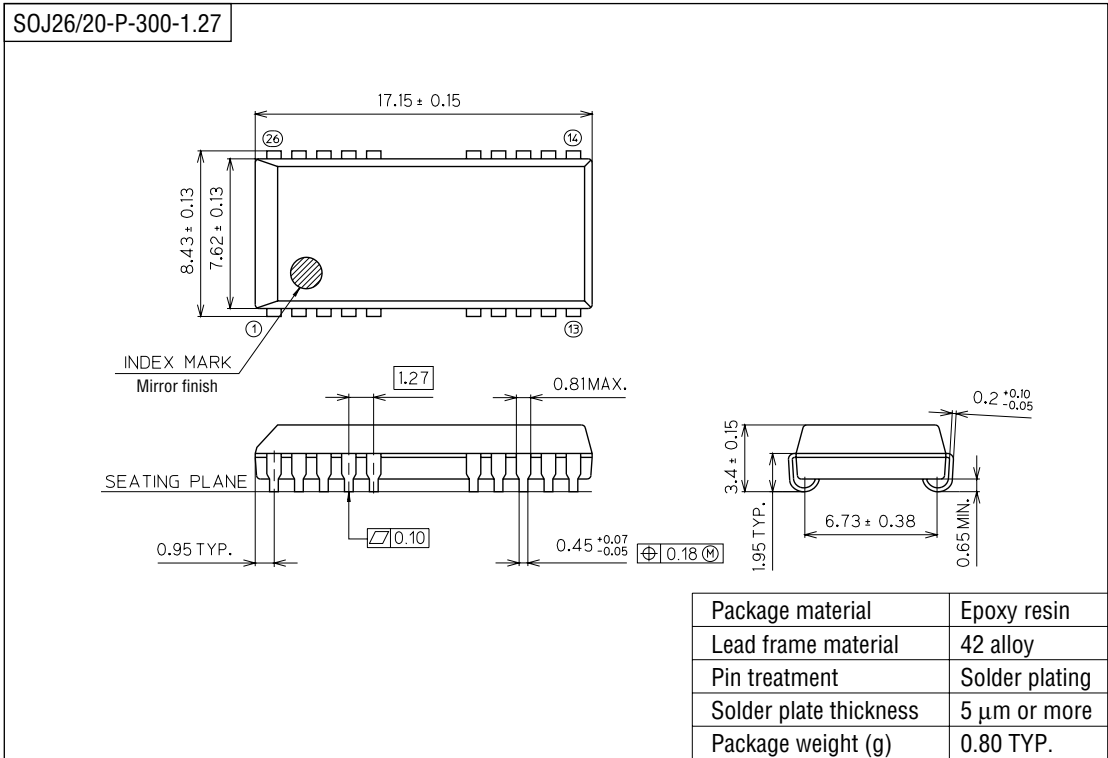


Hidden Refresh Write Cycle



PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

